MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2016/2017

DCS5158 – COMPUTER ARCHITECTURE

(DIT Students Only)

4 MARCH 2017
2.30 p.m. – 4.30 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENT:

1. This question paper consists of **7** pages with **2** sections.
2. Answer **ALL** questions.
3. For **Section A**, shade your answers on the OMR sheet provided.
4. For **Section B**, write your answers in the answer booklet provided.

SECTION A: MULTIPLE CHOICE QUESTIONS (MCQ) (20 Marks)

Instruction: *Answer **ALL** the questions in this section and shade your answers on the OMR sheet provided.*

1. Which of the following are **TRUE** about the structural components of a computer?
   I. Main memory to store data.
   II. Operating system to perform the data processing function.
   III. I/O to move data between the computer and its external environment.
   IV. System interconnection to provide the communication among the components.

   A. I, II and III
   B. I, II and IV
   C. I, III and IV
   D. All of the above

2. Which of the following specifies the address in memory of the word to be written from or read into the memory buffer register?
   A. Program counter
   B. Accumulator
   C. Instruction register
   D. Memory address register

3. Which of the following are the factors contributing to the replacement of vacuum tubes by transistors?
   I. Smaller
   II. Cheaper
   III. Dissipates less heat
   IV. Faster

   A. I, II and III
   B. I, II and IV
   C. I, III and IV
   D. II, III and IV

4. Which of the following is the least significant digit of 6935_{10}?
   A. 6
   B. 9
   C. 3
   D. 5

Continued...

5. What is -78_{10} in one's complement with 8-bit representation?
   A. 01001110_2
   B. 10110001_2
   C. 10110010_2
   D. 11001110_2

6. Which of the following is the value of $6E.8FA_{16}$ in binary representation?
   A. 1111110.100011111011_2
   B. 1111111.100011111011_2
   C. 1101110.100011111010_2
   D. 1101111.100011111010_2

7. Which of the following is the value of 767634_8 in decimal representation?
   A. 257948_{10}
   B. 257884_{10}
   C. 257949_{10}
   D. 257885_{10}

8. Which of the following instructions is applicable to a special memory organization called a stack?
   A. Zero-address
   B. One-address
   C. Two-address
   D. Three-address

9. _____ instructions change the format or operate on the format of data.
   A. Arithmetic
   B. Logical
   C. Conversion
   D. Transfer of control

10. Which of the following is the postfix notation for (G + P) * (E – M / S) + E?
    A. G P E M S E + * – / +
    B. G P + E M S / – * E +
    C. G P + * E M S – / E +
    D. G P + E M S * – / E +

Continued...

11. Which of the following is **TRUE** about Programmable ROM?
    A. Can be written into at any time without erasing prior contents.
    B. Requires periodic charge refreshing to maintain data storage.
    C. Nonvolatile and may be written into only once.
    D. Erasure is performed by shining an intense ultraviolet light through a window that is designed into the memory chip.

12. Which of the following are the advantages of the use of glass substrate in magnetic disk?
    I. Ability to support lower fly heights.
    II. Better stiffness to reduce disk dynamics.
    III. Minimize memory writes.
    IV. Greater ability to withstand shock and damage.

    A. I and II
    B. I, II and IV
    C. I, III and IV
    D. All of the above

13. _____ is also used to address I/O ports in which the higher-order bits are used to select a particular module on the bus, and the lower-order bits select a memory location or I/O port within the module.

    A. Control bus
    B. Operation bus
    C. External bus
    D. Address bus

14. _____ is a bus located outside a CPU chip for connecting the rest of the system components to the CPU.
    A. External bus
    B. Data bus
    C. Peripheral bus
    D. Internal bus

15. The method of accessing the I/O devices by repeatedly checking the status flags is _____.
    A. memory-mapped I/O
    B. programmed I/O
    C. interrupt-driven I/O
    D. direct memory access

Continued...

16. The I/O function includes _____ to coordinate the flow of traffic between internal resources and external devices.
    A. data buffering
    B. device communication
    C. control and timing
    D. processor communication

17. In the following statement, ***X*** is referred to _____ technique.

> ***X*** *is impractical to dedicate more than a few bus lines or processor pins to interrupt lines.*

    A. software poll
    B. multiple interrupt lines
    C. daisy chain
    D. bus arbitration

18. All of the following are **TRUE** about factors that limit the performance enhancement of pipelining, **EXCEPT** _____.
    A. The stages are not of equal duration.
    B. Conditional branch instruction which can invalidate several instruction fetches.
    C. All instructions are of equal duration.
    D. Unpredictable event such as interrupt.

19. Which of the following is **FALSE** about high-level programming languages (HLLs) with regards to execution of machine instructions?
    A. It allows the programmer to express algorithms more concisely.
    B. It allows the compiler to take care of details that are not important in the programmer's expression of algorithms.
    C. It often supports naturally the use of structured programming and/or object-oriented design
    D. It is difficult to implement pipelining with HLLs.

20. Which of the following are types of data hazard?
    I. Read after write (RAW), or true dependency
    II. Write after read (WAR), or antidependency
    III. Write after write (WAW), or output dependency
    IV. Read after read (RAR), or true dependency

    A. I, II and III
    B. I, III and IV
    C. II, III and IV
    D. All of the above

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SECTION B: STRUCTURED QUESTIONS (80 Marks)

Instruction: *Answer **ALL** the questions in this section and write your answers in the answer booklet provided.*

QUESTION 1 (20 Marks)

a) Assume that currently the Program Counter (PC) holds 801H. Execute the first **FIVE (5)** instructions starting from 801 and show the contents of the registers (PC, AC and IR) and any changes made to the memory at the end of each instruction. The original memory contents, relevant instructions with their meanings are given below.

[10 Marks]

Address	Content
801	1912
802	5911
803	6910
804	5913
805	2910
...	...
910	1CC6
911	2DE5
912	C3AB
913	161E
...	...

Original memory contents

Instruction	Meaning
0001	Load AC from memory
0010	Store AC to memory
0101	Add to AC from memory
0110	Subtract memory from AC

Partial list of opcodes

b) Use an 8-bit binary representation (2's complement) to show how $78_{10} - 115_{10}$ is calculated. Verify the result. [5 Marks]

c) Perform the following conversions. All the necessary steps to obtain the answers must be shown.

i. Convert $5C8E.6F9_{16}$ to its octal equivalent. [3 Marks]
ii. Convert 9596_{10} to its octal equivalent. [2 Marks]

Continued...

QUESTION 2 (20 Marks)

a) Given the following expression,

$$Z = [((R - E) * M) / T + U] * [K + D / (B / S)]$$

i. Convert the expression to postfix notation. [1 Mark]

ii. Write the following machine instructions:

- Zero-address [2 Marks]
- One-address [2 Marks]
- Two-address [2 Marks]

iii. Draw the stack diagrams that illustrate the program execution. [3 Marks]

b) A computer system has a memory architecture made up of main memory of 16GB and cache of 16384KB. In order to perform an efficient mapping function, the main memory is arranged in blocks of 512 bytes.

Draw the address structures for different mapping functions as stated below. Indicate the fields and the number of bits required for each field.

i. Direct Mapping [3.5 Marks]

ii. Sixteen-Way Set Associative Mapping [3.5 Marks]

iii. Associative Mapping [3 Marks]

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QUESTION 3 (20 Marks)

a) With the aid of diagrams, differentiate between direct addressing and register addressing techniques. Give **ONE (1)** advantage for each addressing technique. [8 Marks]

b) From a user's point of view, the two most important characteristics of memory are capacity and performance. List and briefly explain **THREE (3)** parameters that are used in measuring performance of memory. [6 Marks]

c) Briefly explain **THREE (3)** characteristics of bus system. [6 Marks]

QUESTION 4 (20 Marks)

a) In pipelining, the instruction processing could be decomposed to six stages to gain further speedup. State and explain any of the **FIVE (5)** stages in a six-stage pipeline. [5 Marks]

b) Given **SIX (6)** instructions where each instruction has **FIVE (5)** stages (FI, DI, CO, EI and WO) with delays of 4, 5, 3, 4 and 5 seconds for each stage respectively.

i. Draw a timing diagram for instruction pipeline operation. [5 Marks]

ii. Calculate the **total processing time**, **speedup** and **throughput** for the implementation of pipelining and non-pipelining. [10 Marks]
[Note: Please write the formula that is appropriate to use]

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